A GENERAL CAD TOOL FOR LARGE-SIGNAL GaAs MESFET CIRCUIT DESIGN

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ABSTRACT

An accurate and general CAD tool for large-signal GaAs MESFET design has been developed. It is based upon incorporation of an accurate GaAs MESFET model in the SPICE circuit simulation. The tool has been utilized in the analysis of microwave power amplifiers, oscillators and mixers, and GaAs digital IC's. Examples of some of these studies are presented.

INTRODUCTION

Gallium Arsenide MESFETs are being utilized in an increasing number of microwave, millimeter-wave and high speed digital circuits. Many of these circuits involve large-signal behavior, and so cannot be described by small-signal models or with simple frequency-domain circuit simulations. Despite the growing importance of GaAs devices in large-signal applications, no general design techniques for these circuits has yet emerged. Instead, the designer of non-linear circuits is often forced to use tedious, measurement intensive techniques such as load-pull or large-signal S-parameter characterization. This vacancy has impeded the growth in our understanding of the non-linear device-circuit interactions which can be critical to system performance.

Difficulties involved in large-signal system design are further complicated by the trend toward monolithic circuitry. Although monolithic circuits offer many potential cost and performance advantages, they also make the task of individually characterizing either the device or circuit more difficult.

The present work incorporates an accurate device model which is derived primarily from physical parameters (ie. device geometry and material characteristics) with the general time-domain circuit simulation package, SPICE. This combination allows the analysis of a wide variety of both linear and non-linear circuits to be performed with a minimum expenditure of programming effort. Because of the physical basis of the device model used, it also enables the designer to optimize the device and circuit simultaneously. This capability makes this tool especially useful in designs involving monolithic technology.

DEVICE MODEL

The device model used for this work is based on the model of Lehovec and Zuleeg [2] with some modifications to improve its accuracy. It is designed to simulate JFETs and MESFETs with micron and submicron dimensions. The device performance is predicted from fabrication controlled physical parameters including device dimensions, channel doping density, mobility and pinch-off potential. In addition, when extreme precision is required, more accurate model results may be obtained by the inclusion of optional empirical expressions for output conductance, device capacitance and subthreshold currents.

Modeled results have been compared to measurements made on a number of different devices. Shown in Figure 1 are measured and modeled I-V characteristics for a 1-micron gate length ion-implanted MESFET. The agreement is good in both the normal and subthreshold regions of operation. This latter result can be of critical importance in the analysis of GaAs ICs for digital applications.

In large-signal time-domain simulations, it is important not only that steady-state current-voltage relationships be accurately described, but that the device capacitances also be represented correctly. The results of the device model used in this work have been compared to the capacitance predictions of an accurate two-dimensional simulation. The results, shown in Figure 2, indicate excellent agreement. For Figure 2,

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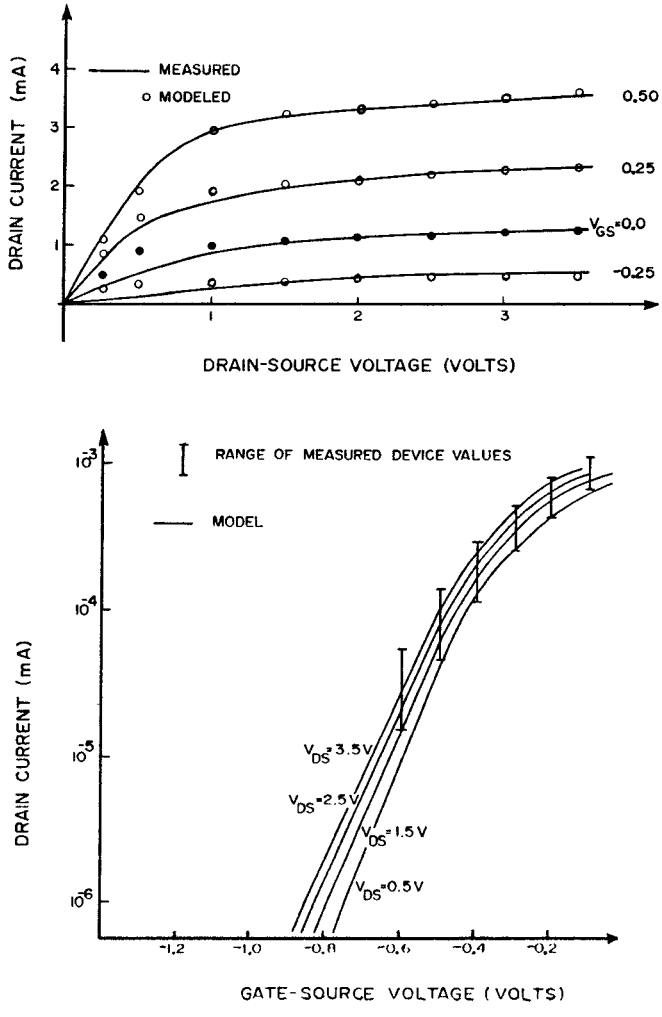


Figure 1) Measured and modeled I-V characteristics for a 1-micron device. a) Drain current as a function of drain-source voltage. b) Drain current as a function of gate-source voltage in the subthreshold region.

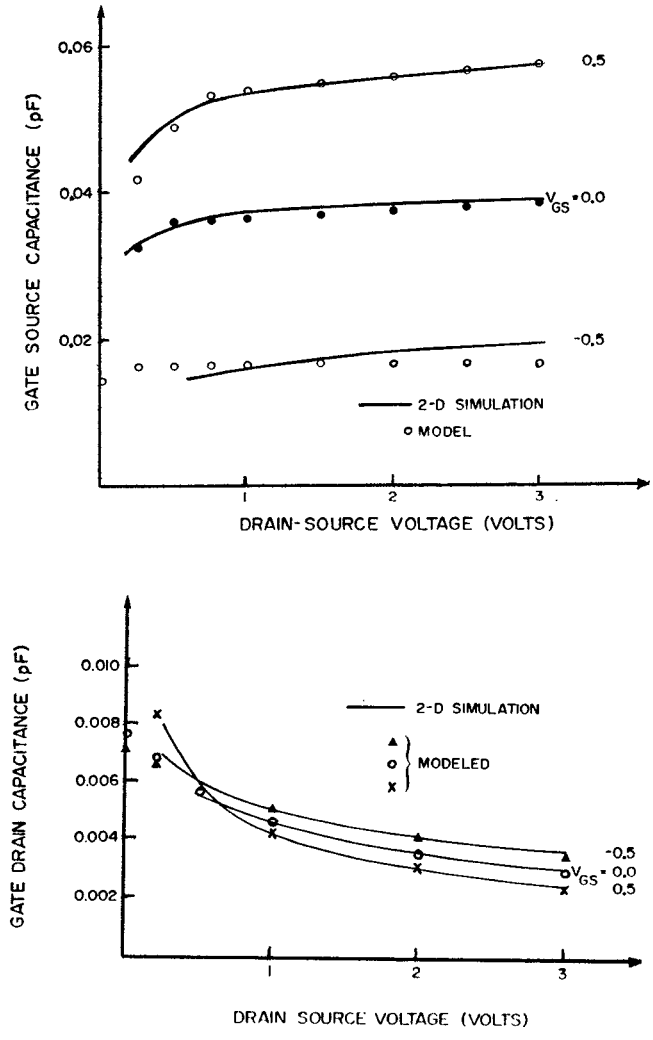


Figure 2) Comparison of device capacitance modeled by simple empirical expressions of the device model and computed by two-dimensional simulations. a) Gate-source capacitance. b) Gate-drain capacitance.

optional empirical expressions [4] have been used to achieve the fit.

CIRCUIT SIMULATIONS

The circuit simulation package, SPICE, is a general-purpose program and has been used for a variety of circuit design applications. Although SPICE has been used primarily in the analysis of transient switching circuits, sinusoidal waveforms may also be analyzed. It is possible to consider both general lumped and distributed circuit topologies. For sinusoidal simulations, a Fourier analysis of the output waveform can also be specified. Thus, the harmonic output power versus incident power for a power-amplifier circuit can easily be computed. The prediction of conversion gain of MESFET mixers or the output power of an FET oscillator is also easily obtained. Care must be taken, however, when using SPICE to obtain rf behavior predictions. As an example, the FET device described by Willing et al. [1] was simulated with the modified SPICE program. Figure 3 shows the circuit simulated as well as the second and third harmonic content predicted by the technique as a function of waveform periods simulated. It is seen that more than ten periods must be simulated before steady-state is

achieved. For more complicated circuits, it was found to be necessary to simulate as many as thirty periods of the fundamental waveform.

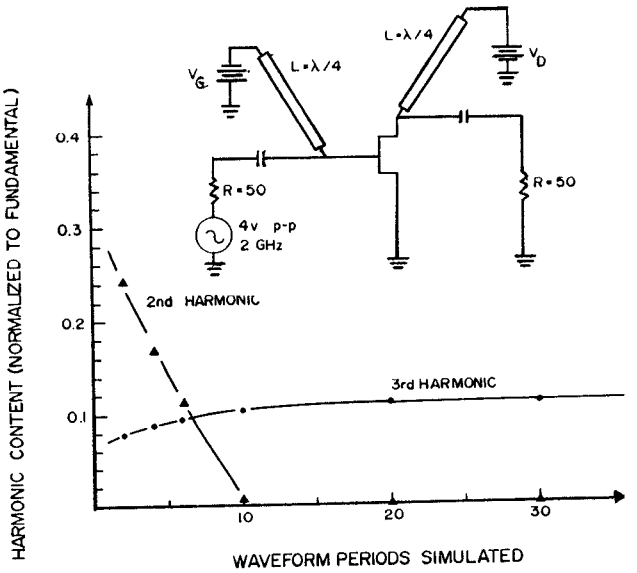


Figure 3) Prediction of the second and third harmonic content for the circuit shown as a function of the number of fundamental waveform periods simulated.

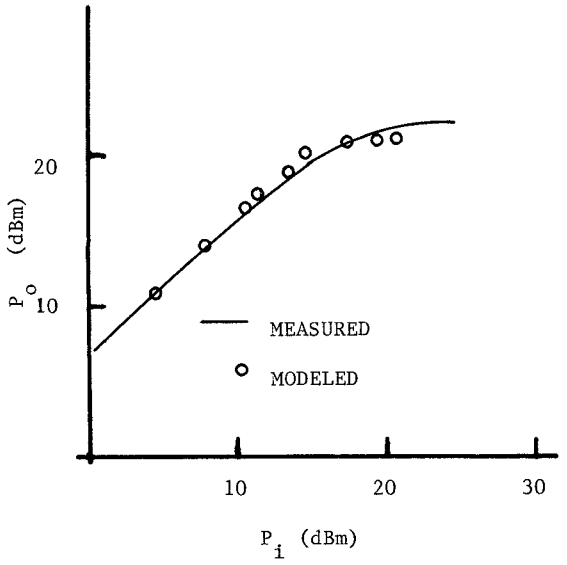
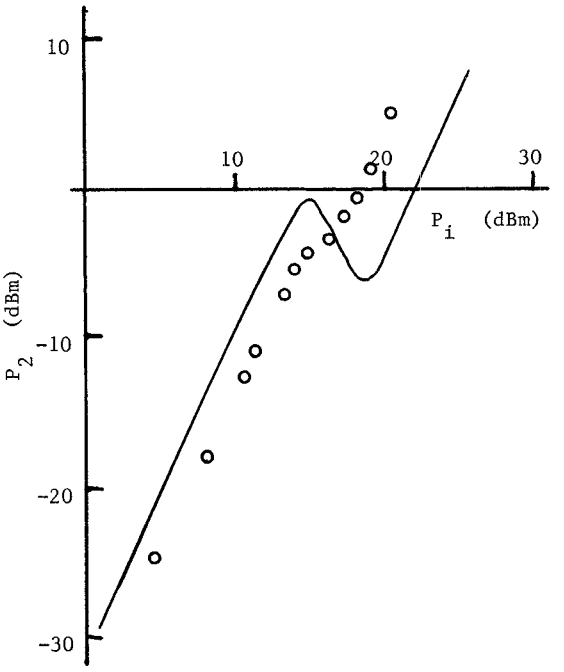


Figure 4) Fundamental output power versus incident power for a GaAs MESFET with a 50 ohm generator and output load. Fundamental frequency is 2 GHz. Measured data is shown by the solid line, modeled results by the points.

The device simulated in Figure 3 was also included in a simulation of the circuit fabricated and measured in that earlier report [1]. Figures 4 and 5 present the results of those simulations. Similar



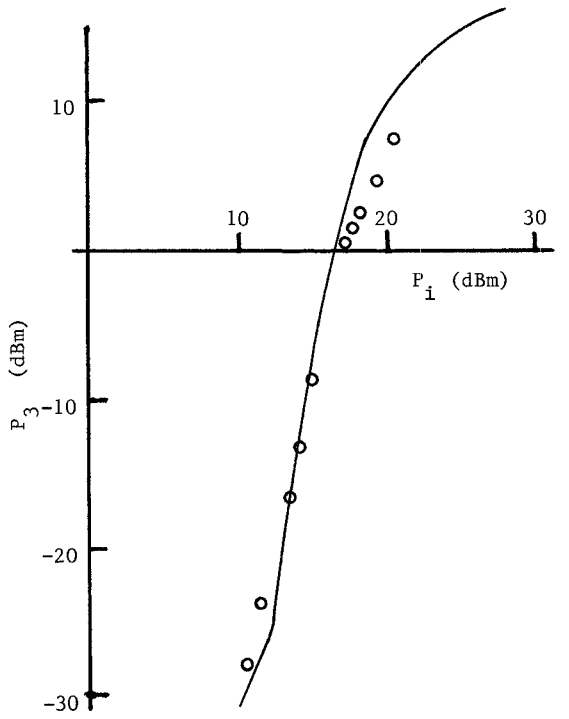


Figure 5) Harmonic output power levels of second and third harmonics versus incident power for the GaAs MESFET of Figure 4. Measured data is shown by the solid line, modeled results by the points.

agreement is also obtained for fourth and fifth harmonic content. The agreement shown in Figures 4 and 5 is obtained without including forward conduction mechanisms in the device model. In cases where conduction through the gate is more critical, it may be included in a first order manner by shunting the transistor input with a diode. This is easily accomplished using the modified version of SPICE described here.

The YIG-tuned FET oscillator circuits described by Trew [5,6] have also been simulated. For these studies, the YIG resonator is modeled as a parallel RLC circuit and the oscillator is excited initially by the application of a pulse to the source of the device. The simulations predict not only bandwidth and output power, but potential problems with fixed bias resonances in the circuit. This information is often difficult to obtain using other oscillator design techniques.

In addition to these analog applications, simulations of GaAs digital ICs can also be accomplished. The dc operating point, transient behavior, and memory cell upset due to radiation events can be analyzed. The modified version of SPICE used in this work was utilized in the simulation of a GaAs memory cell configuration which has been fabricated and used to successfully demonstrate a 256-bit GaAs static RAM [3]. Simulation of the circuit using this modified version of SPICE predicts the DC currents and voltages measured in an actual cell to within 1 percent.

Switching functions have also been simulated for the memory cell circuit as shown in Figure 6. The access time for the circuit has been estimated using SPICE, and the results are in good agreement with measured values.

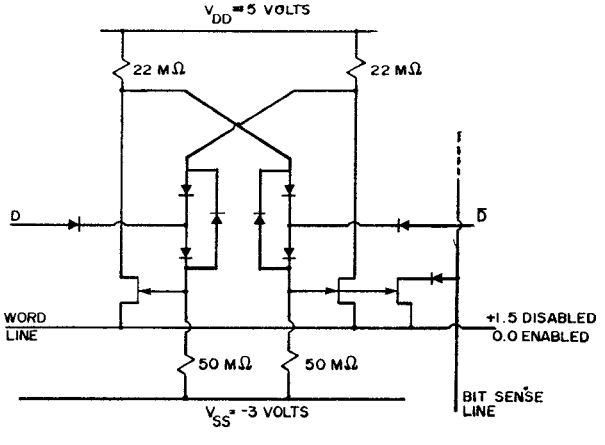


Figure 6) Simulated GaAs memory cell configuration.

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